CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method for modifying a diffusions rate of an impurity implanted in a semiconductor material including steps of

defining a boundary with a structure on a surface of said semiconductor material,

applying a stressed film over said structure and said surface at said boundary, and

annealing said semiconductor material to activate said impurities.

2. The method as recited in claim 1, wherein said structure on said surface of said semiconductor material is a gate structure of a field effect transistor.

3. The method as recited in claim 2, wherein said boundary is defined by a sidewall of said gate structure.

4. The method as recited in claim 3, wherein said sidewall is an offset spacer.

5. The method as recited in claim 3, wherein said sidewall is a source/drain spacer.

6. The method as recited in claim 2, wherein said boundary is defined by a gate electrode of said gate structure.

7. The method as recited in claim 1, further including steps of

implanting extension impurities,

implanting source/drain impurities, and

implanting halo impurities.

8. The method as recited in claim 1 wherein a plurality of said structures are provided on said surface of said semiconductor material, further including a step of

removing said stressed film from a selected said structure prior to said annealing step.

9. The method as recited in claim 8, wherein said plurality of structures include gate structures of pFETs and nFETs.

10. The method as recited in claim 9, wherein said boundary is defined by a sidewall of said gate structures.

11. The method as recited in claim 10, wherein said sidewall is an offset spacer.

12. The method as recited in claim 10, wherein said sidewall is a source/drain spacer.

13. The method as recited in claim 1, wherein said stressed film is a tensile film.

14. An intermediate structure for formation of a semiconductor device, said intermediate structure comprising

a body of semiconductor material including respective regions implanted with boron and arsenic impurities,

a structure on a surface on said body of semiconductor material and forming a boundary, and

a stressed film extending over said structure and said boundary,

wherein when said intermediate structure is annealed to activate said boron and arsenic impurities, a diffusion rate of said boron impurities is modified.

15. The intermediate structure as recited in claim 14, wherein said structure is a gate structure of a field effect transistor.

16. The intermediate structure as recited in claim 15, wherein said gate structure includes a sidewall.

17. The intermediate structure as recited in claim 16, wherein said sidewall is an offset spacer.

18. The intermediate structure as recited in claim 16, wherein said sidewall is a source/drain spacer.

19. An integrated circuit comprising
a pFET, and
an nFET
wherein a boron diffusion concentration profile from extension implants in said pFET corresponds to a lower boron diffusion rate than a boron diffusion rate corresponding to a boron diffusion concentration profile from a boron halo implant in said nFET.

20. A pFET including
a source/drain region formed by implantation with boron, and
an extension region formed by implantation with boron, wherein a boron concentration profile of said extension in a lateral direction differs from a boron concentration in a vertical direction.